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FIG. 1

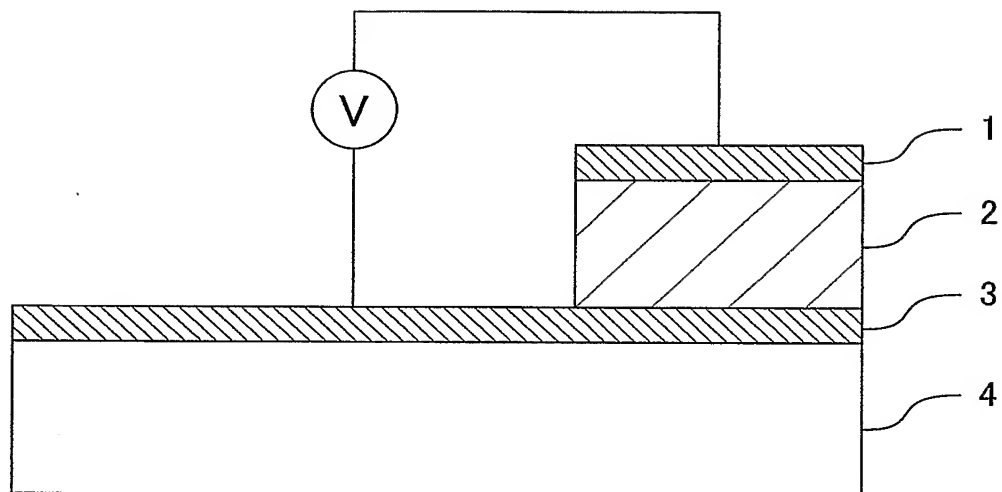


FIG. 2

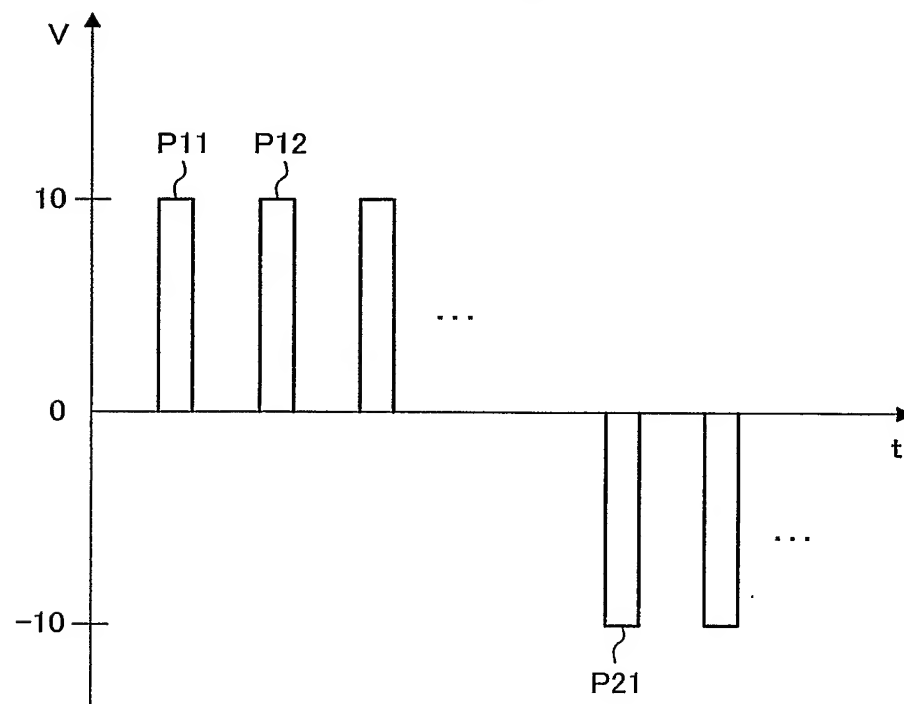
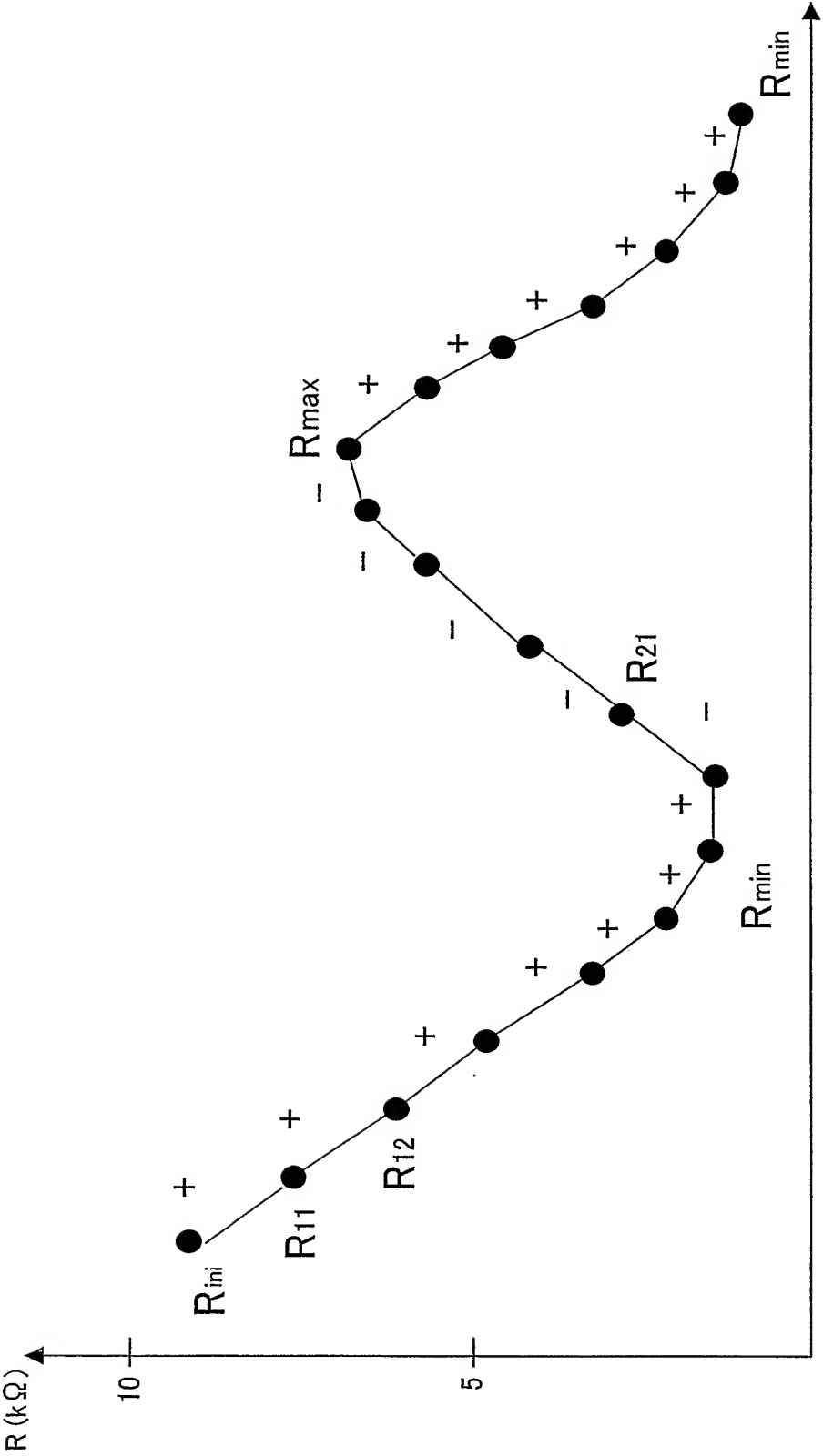


FIG. 3



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FIG. 4

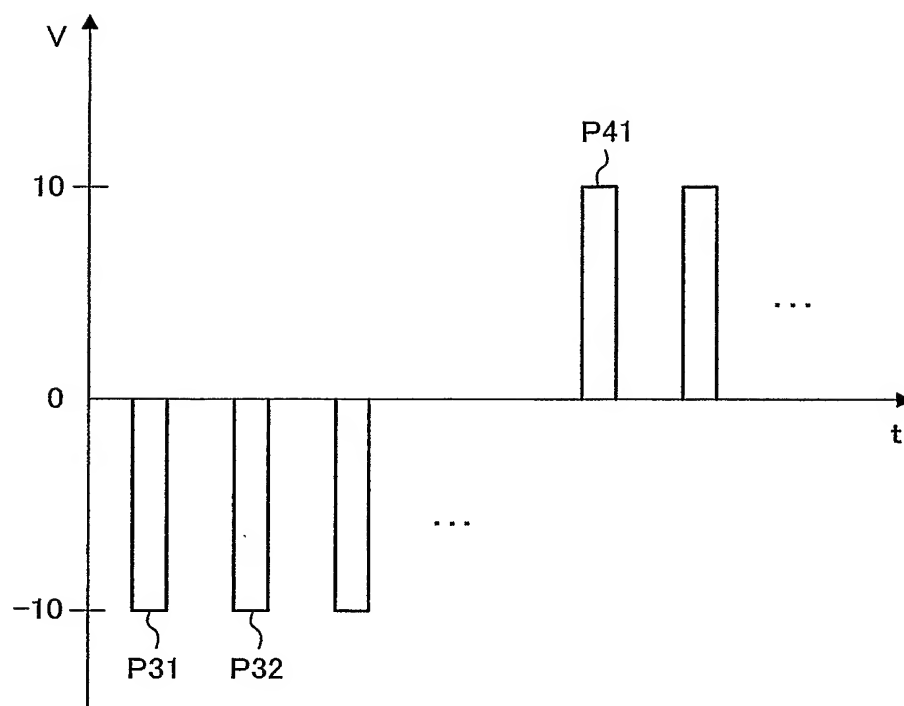
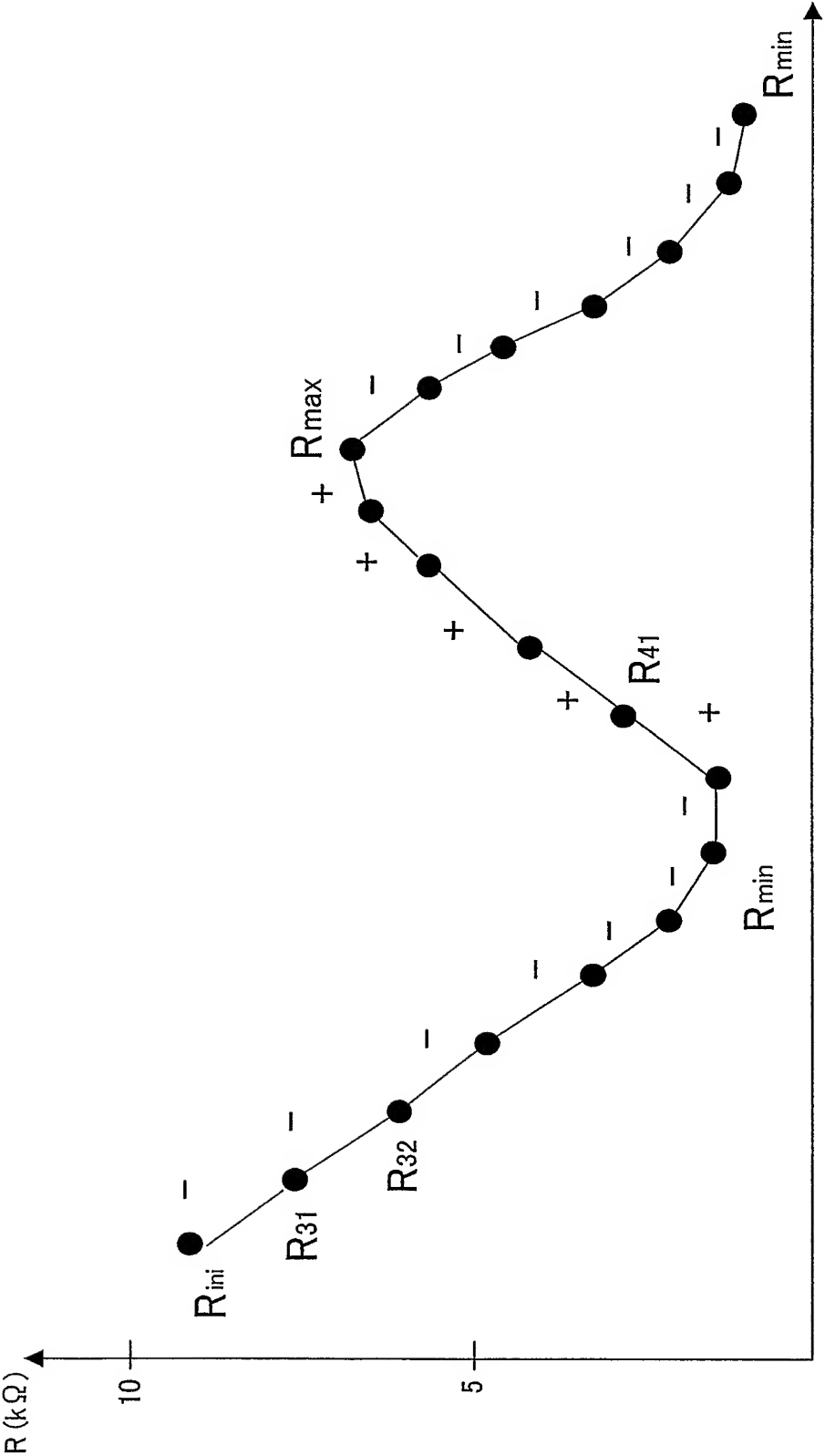


FIG. 5



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FIG. 6

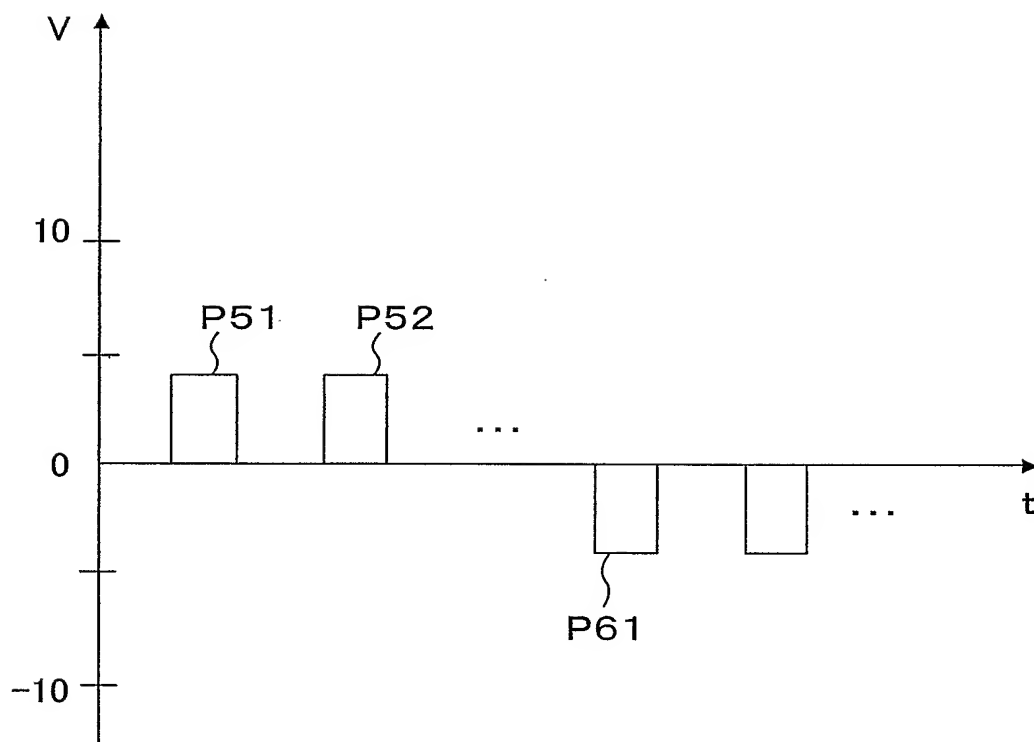
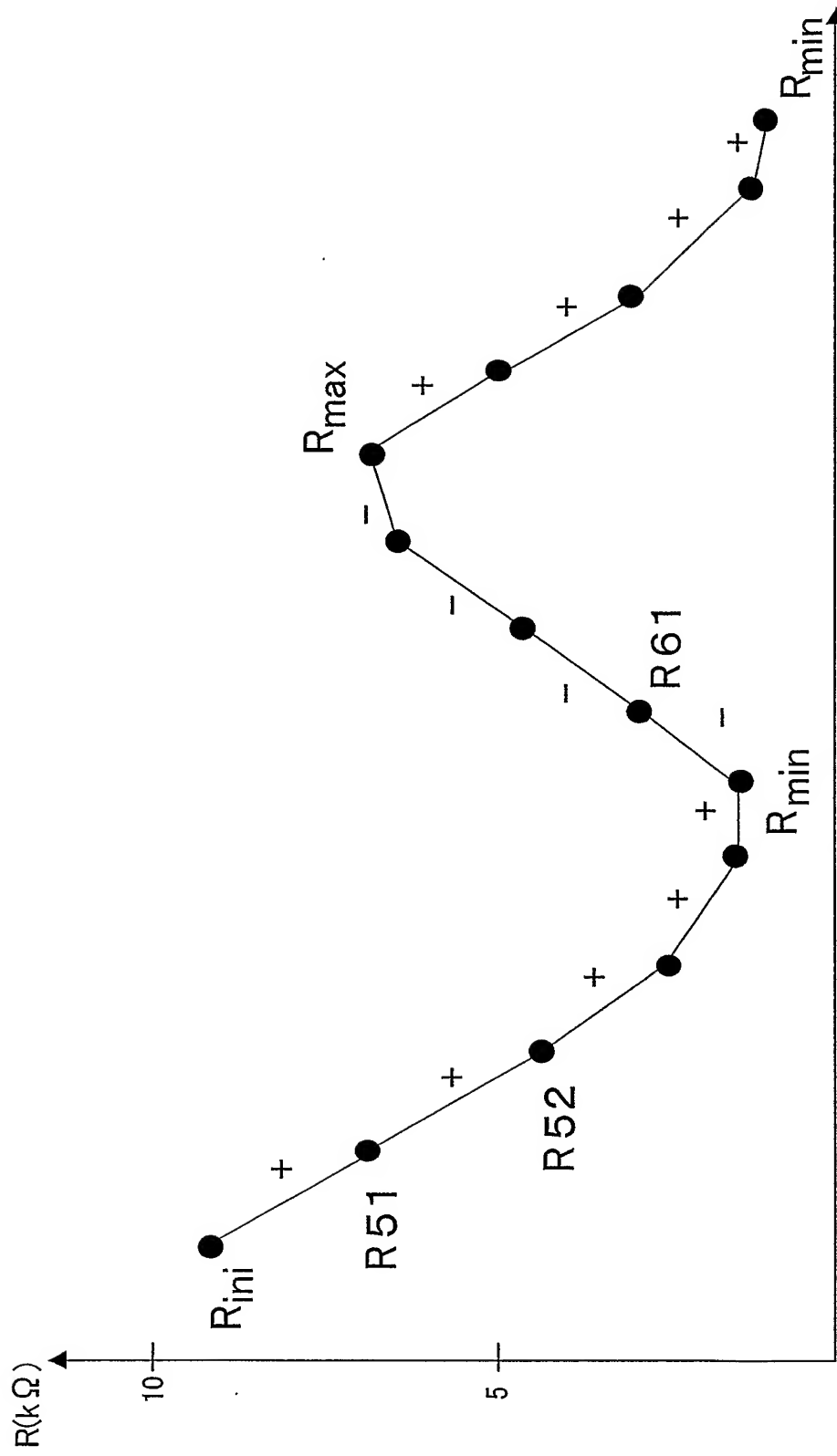


FIG. 7



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FIG. 8

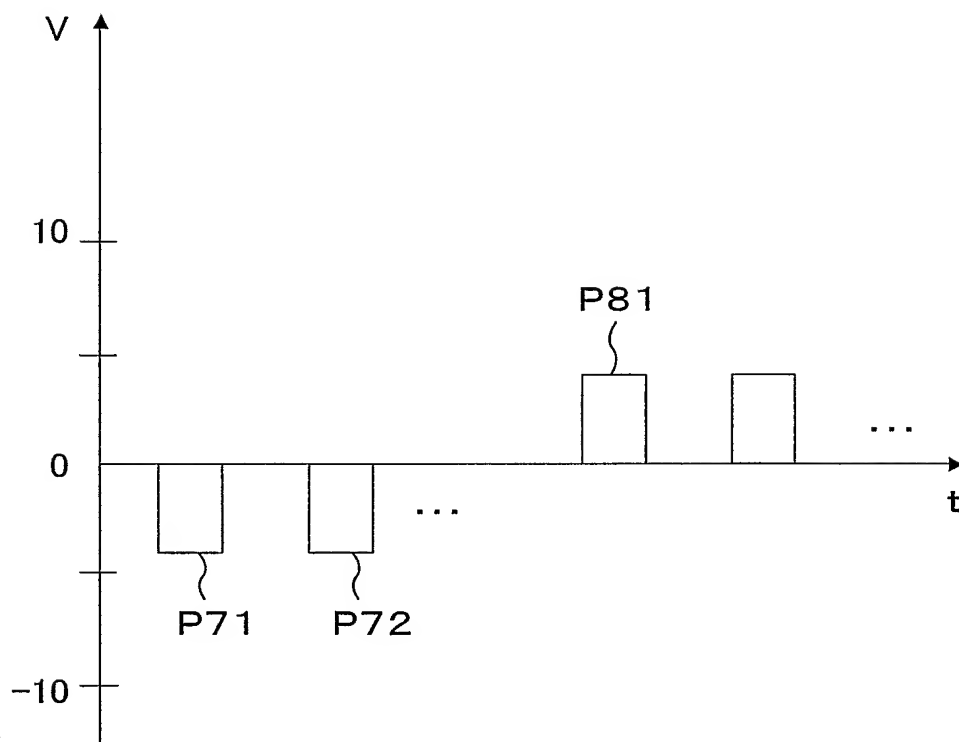
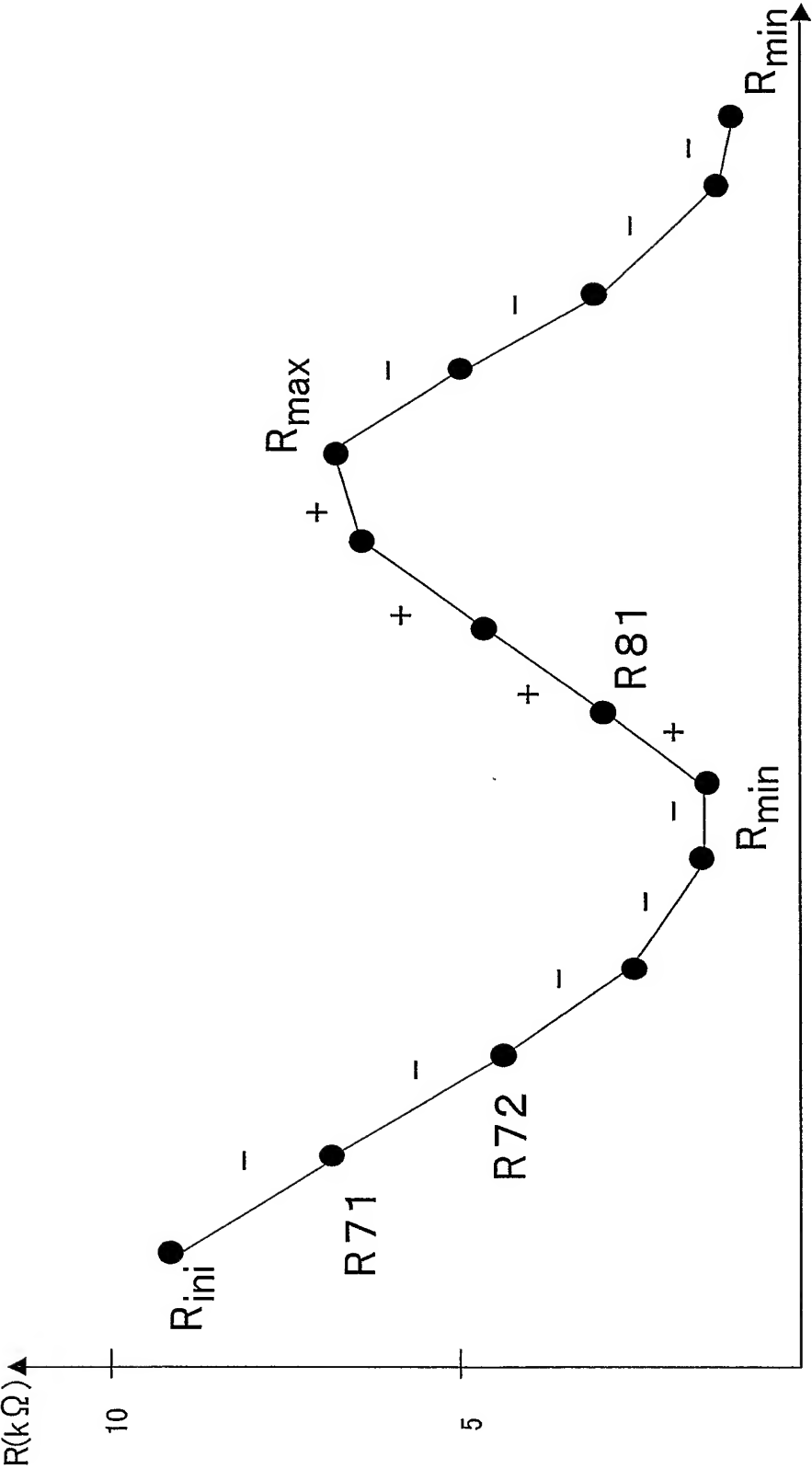
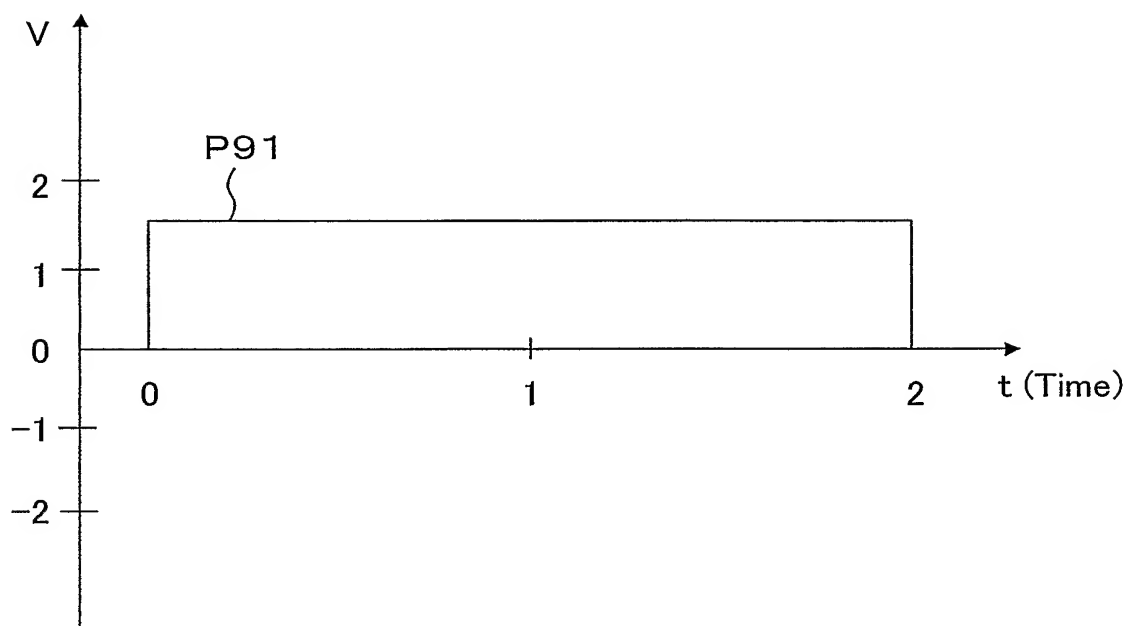


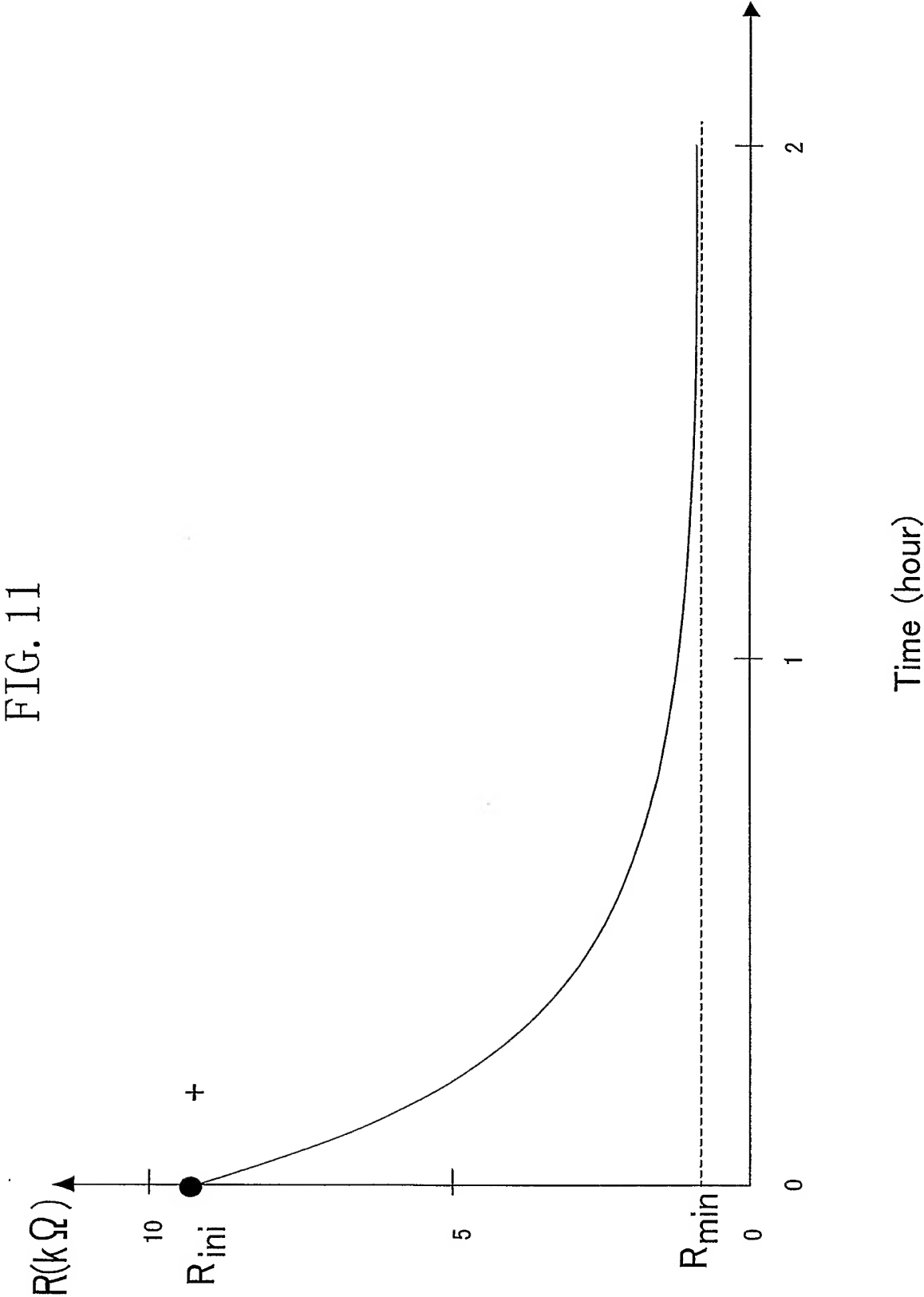
FIG. 9



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FIG. 10





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FIG. 12

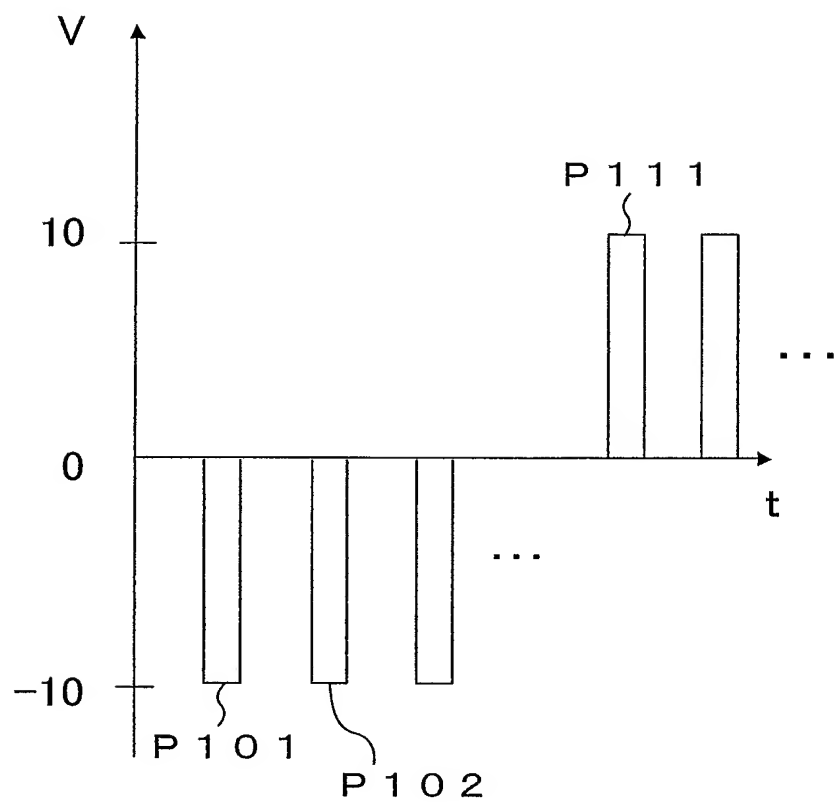
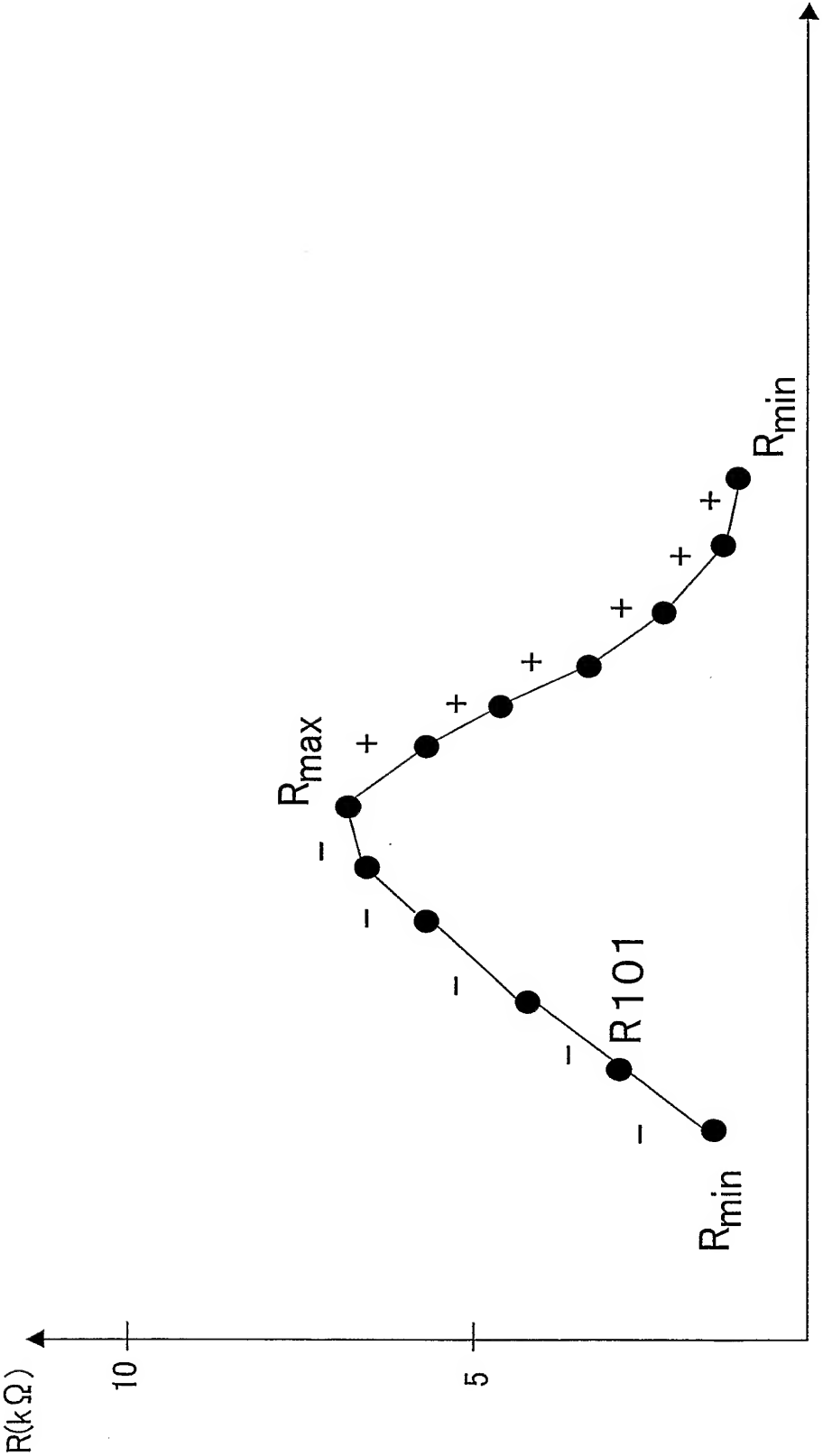
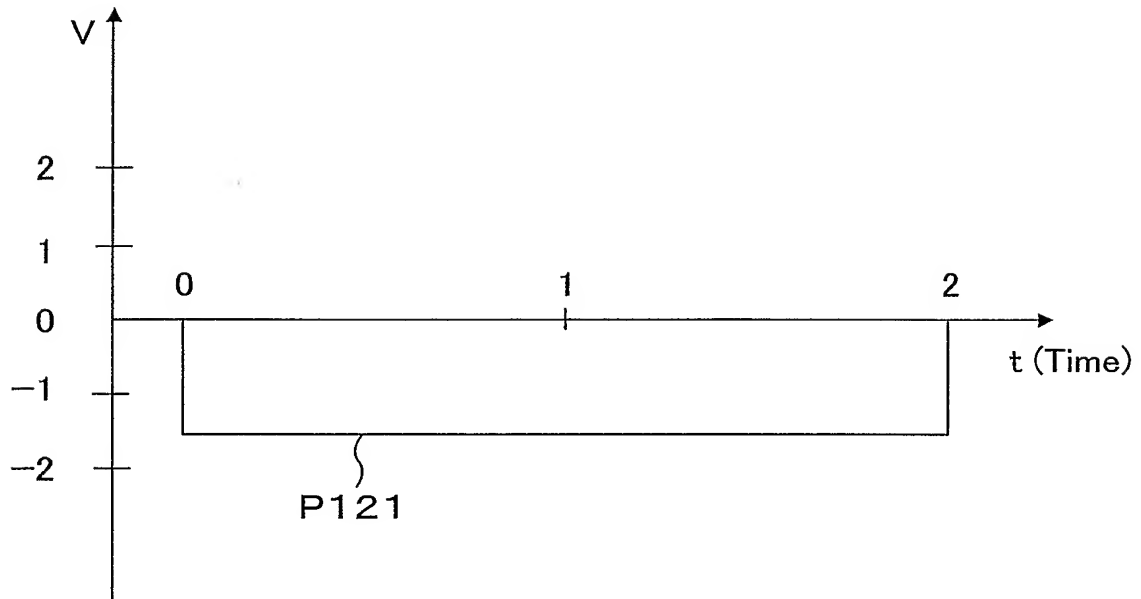


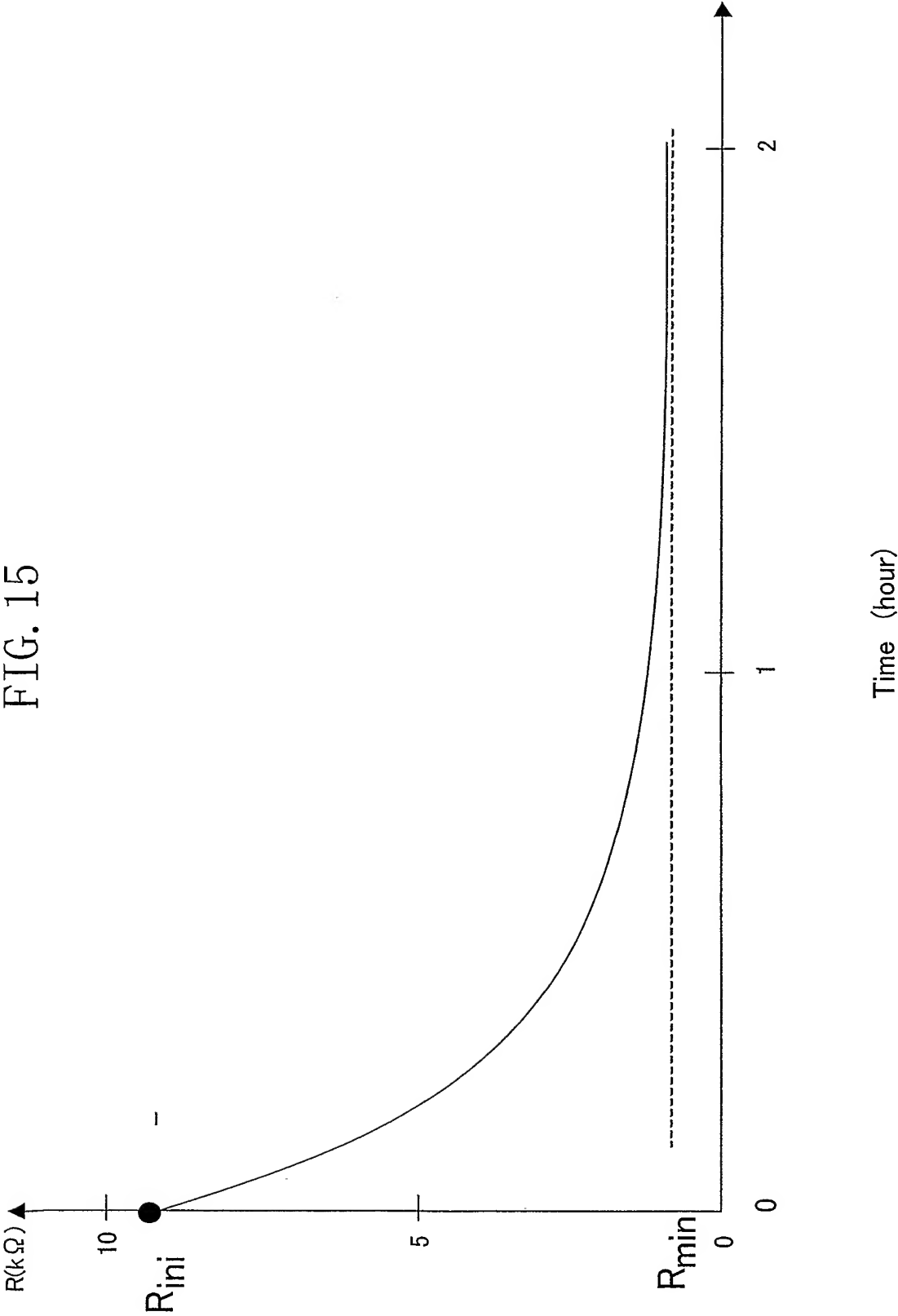
FIG. 13



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FIG. 14





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FIG. 16

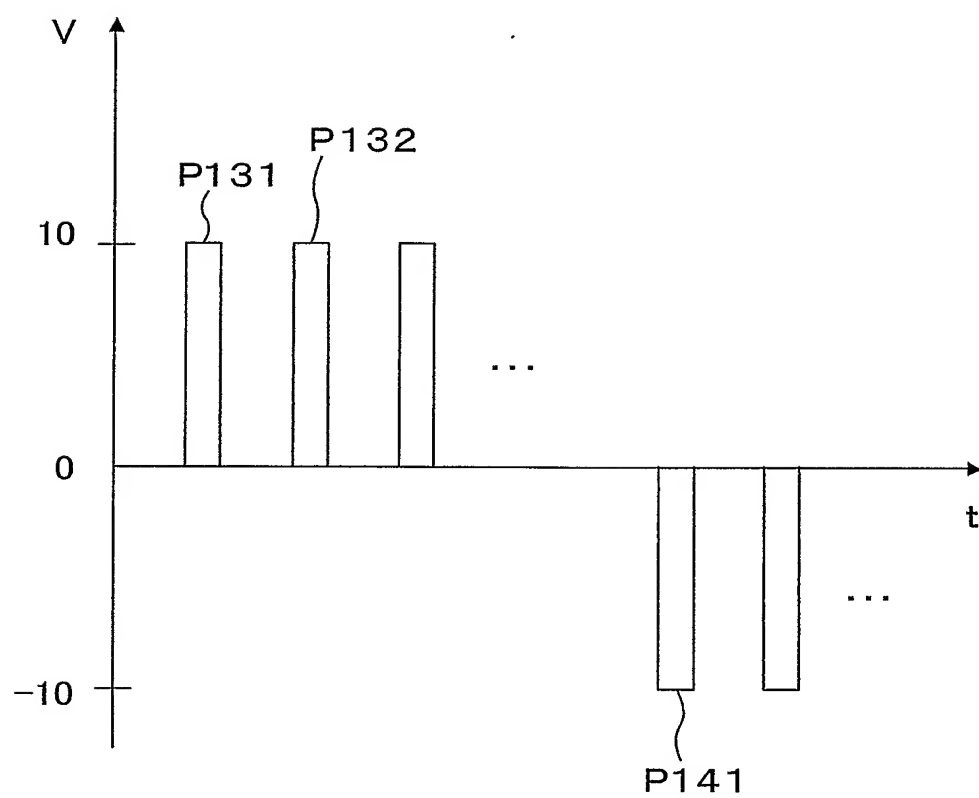
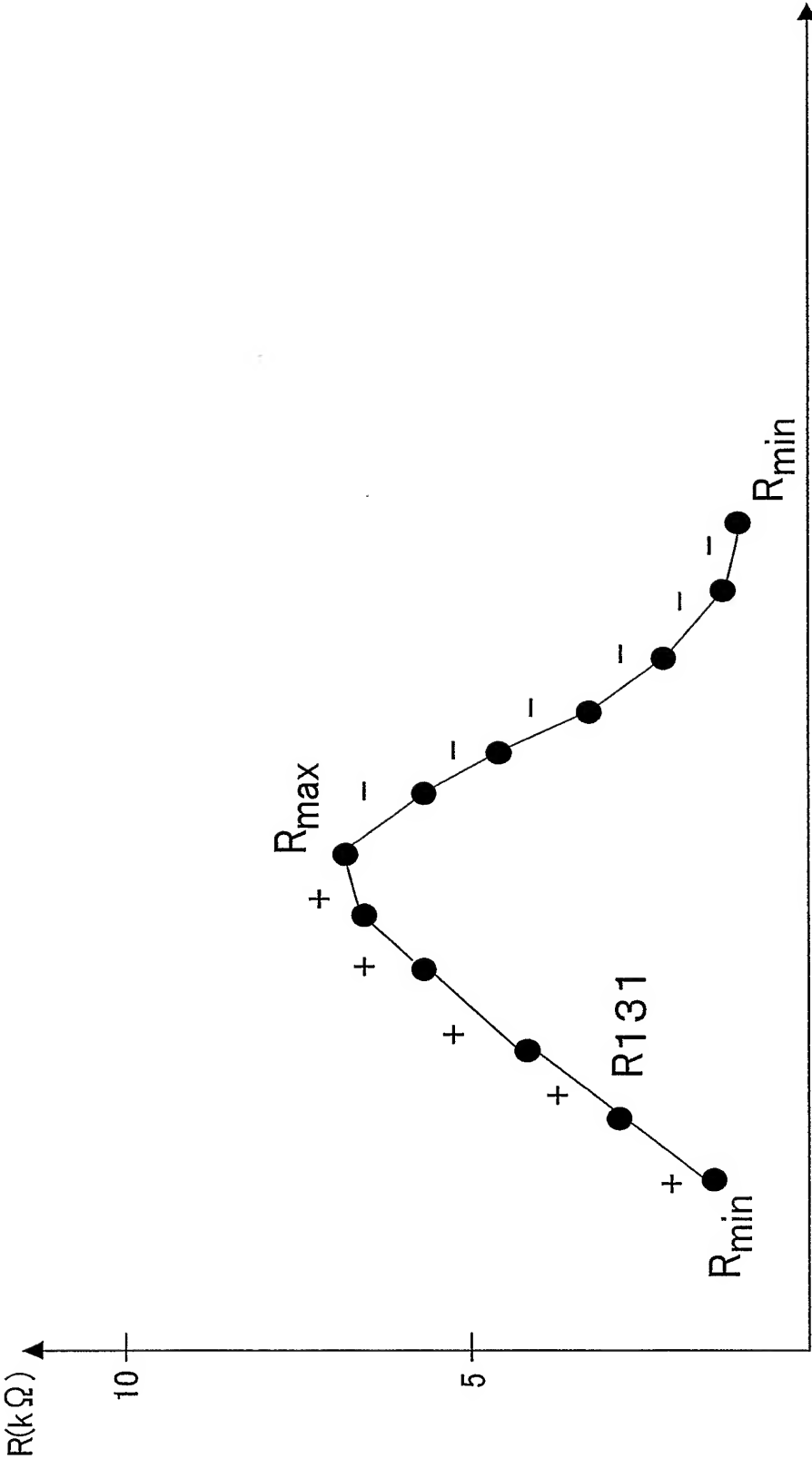
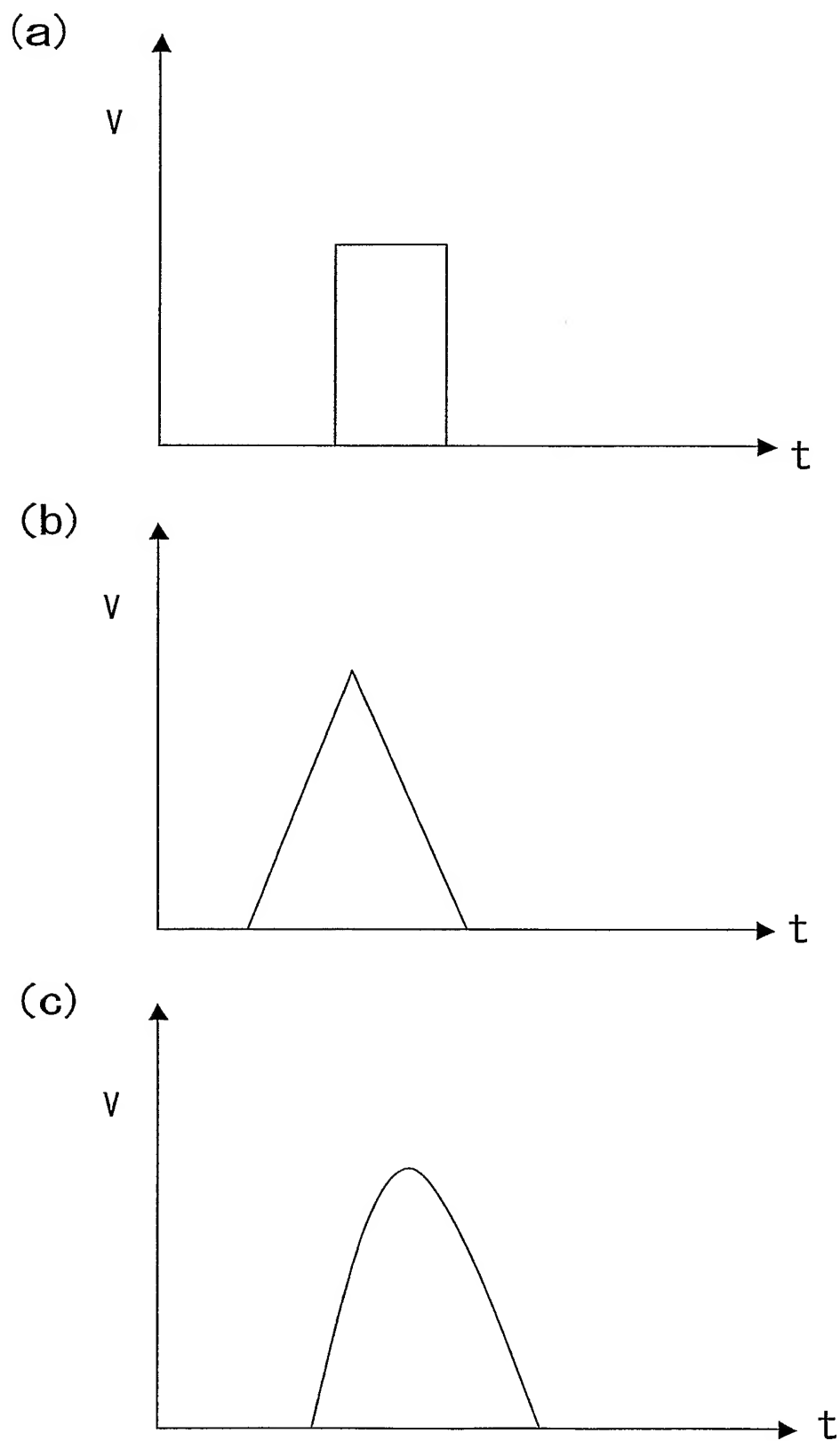


FIG. 17



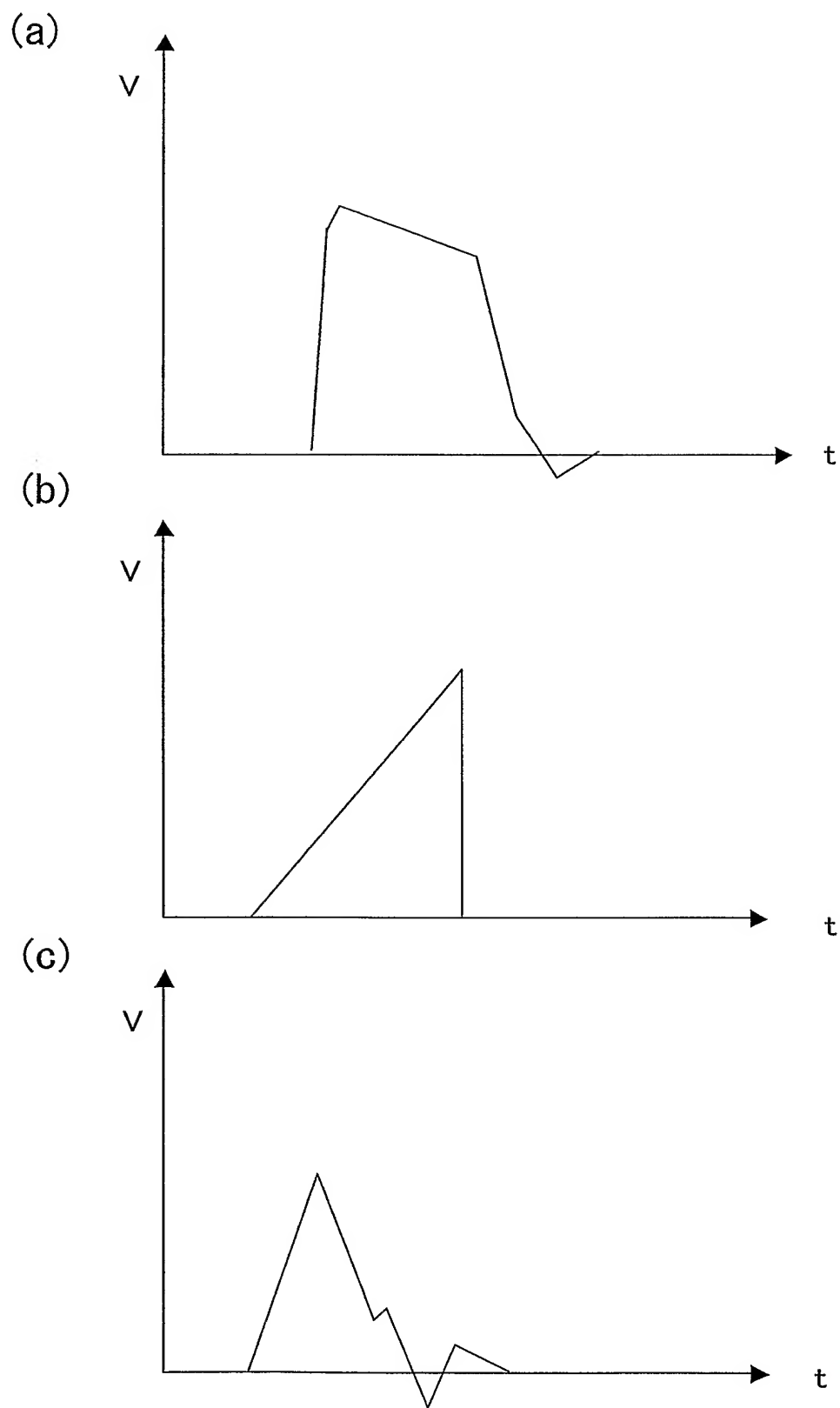
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FIG. 18



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FIG. 19



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FIG. 20

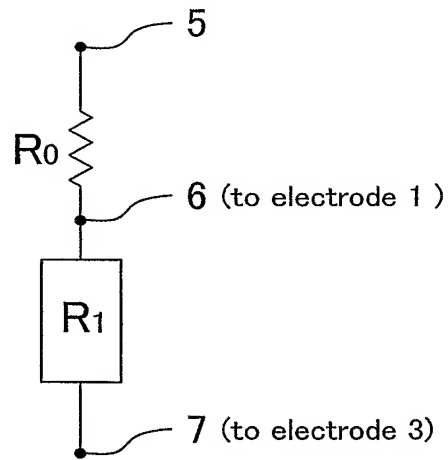
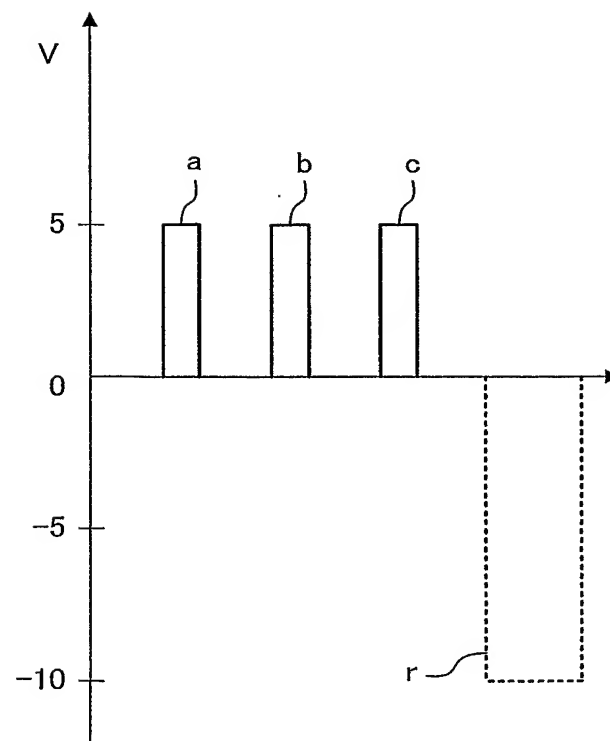


FIG. 21



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FIG. 22

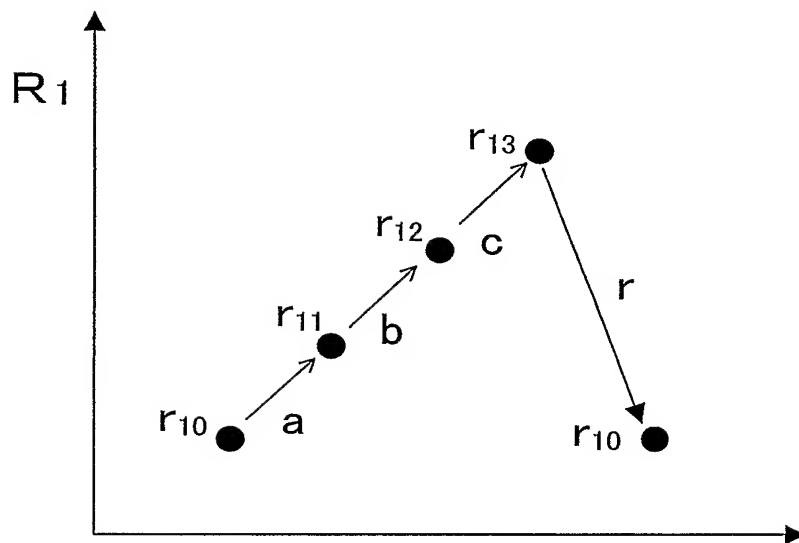
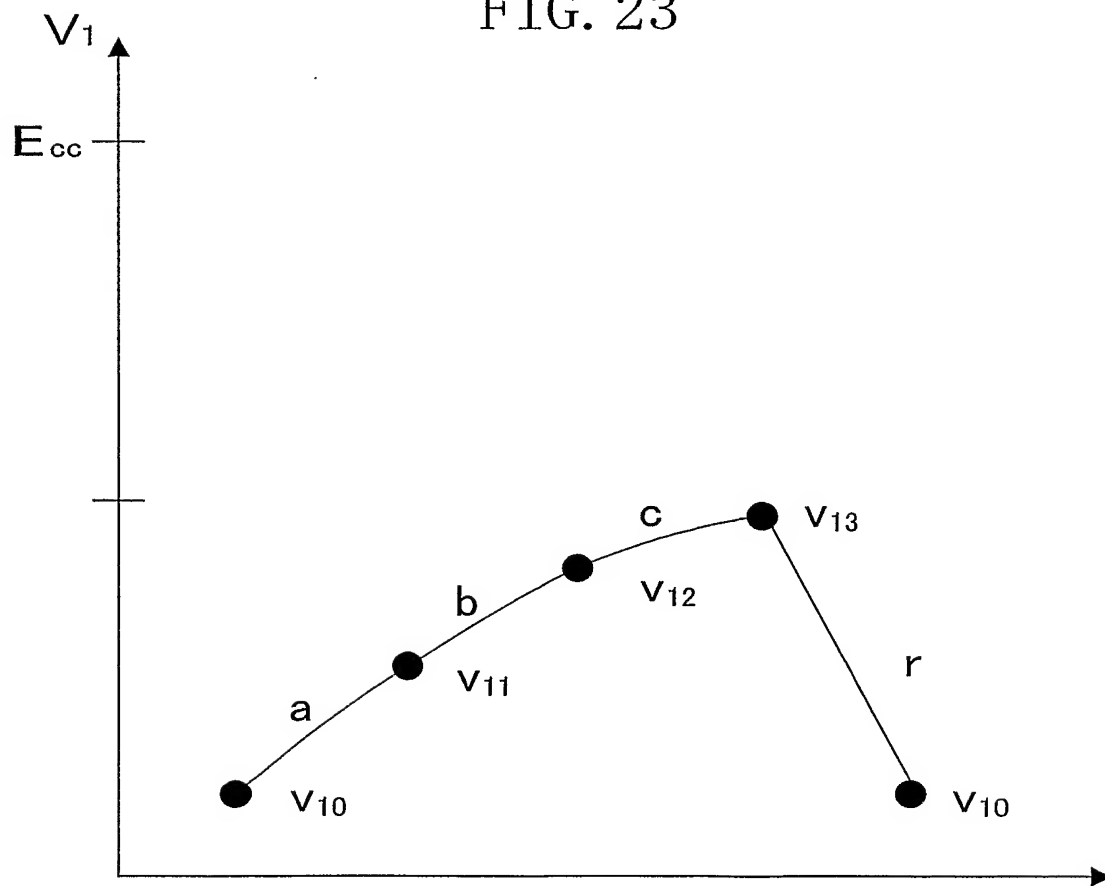


FIG. 23



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FIG. 24

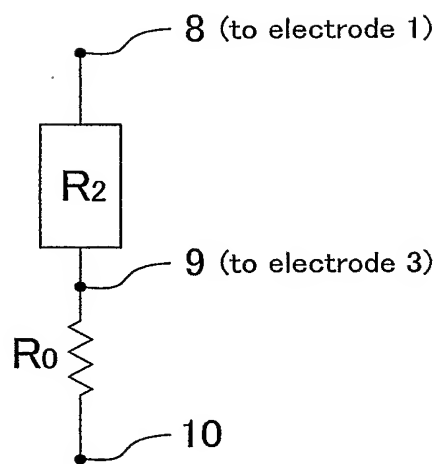


FIG. 25

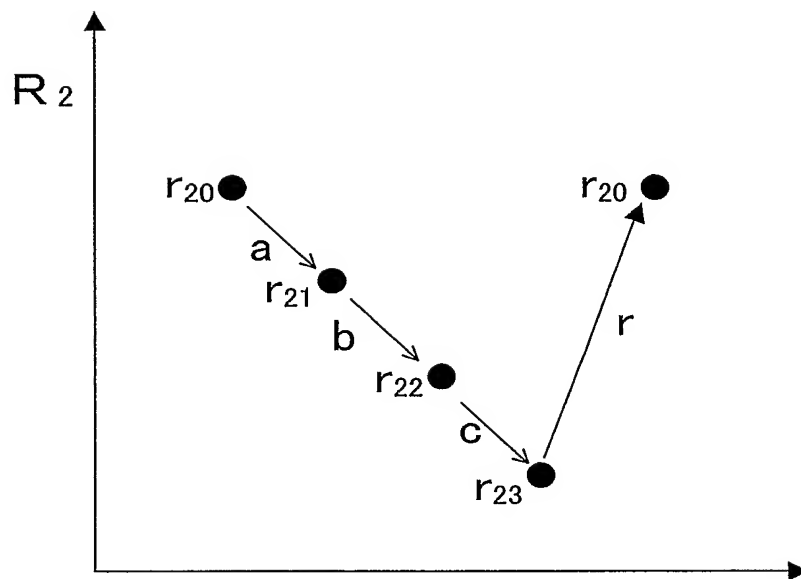
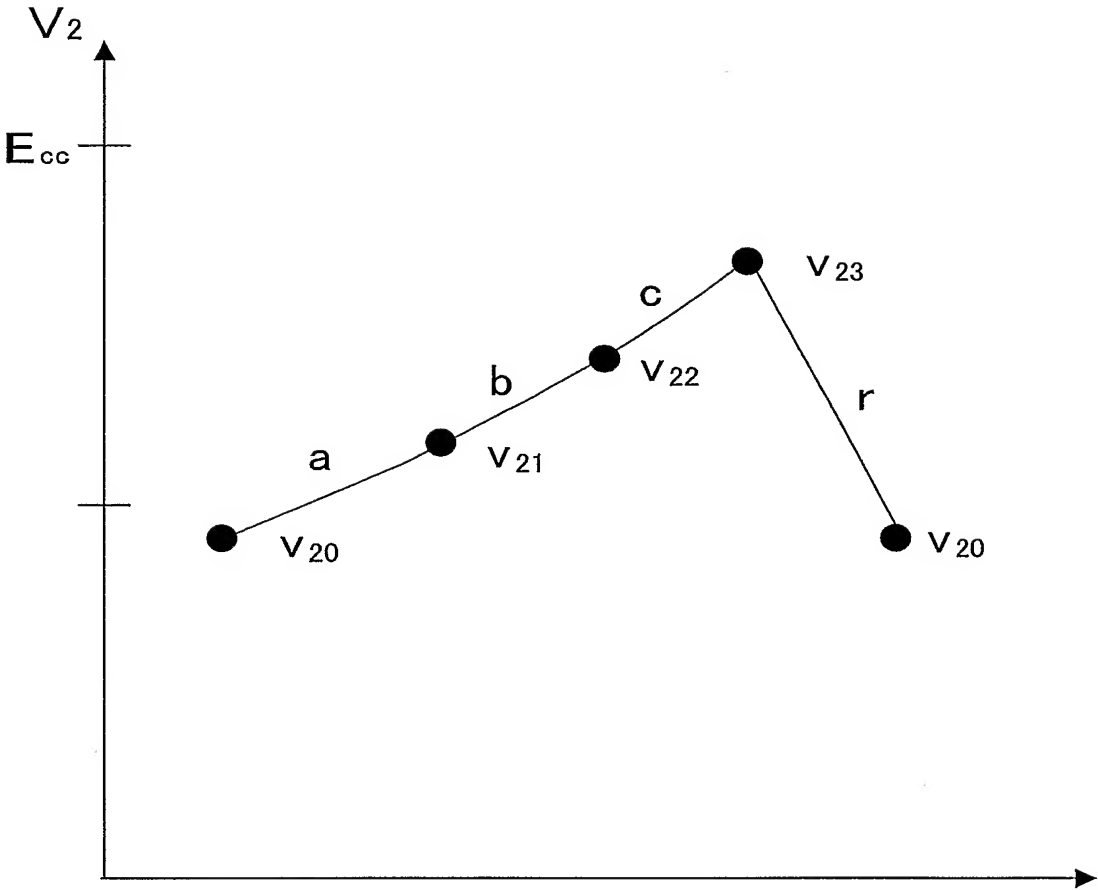
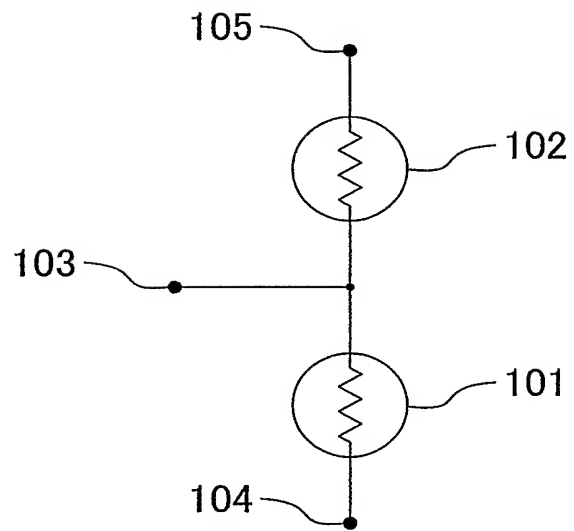


FIG. 26



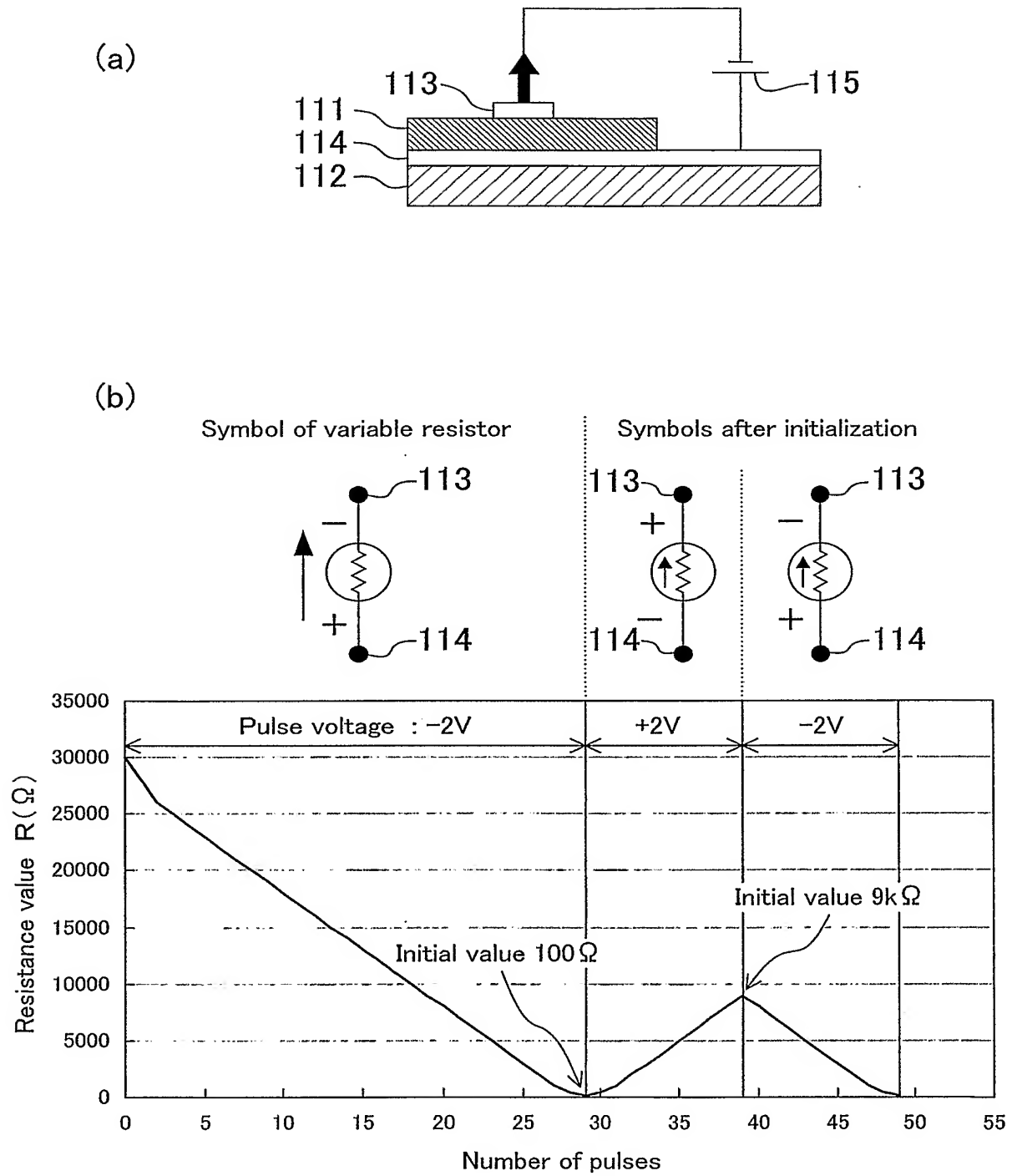
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FIG. 27



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FIG. 28



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FIG. 29

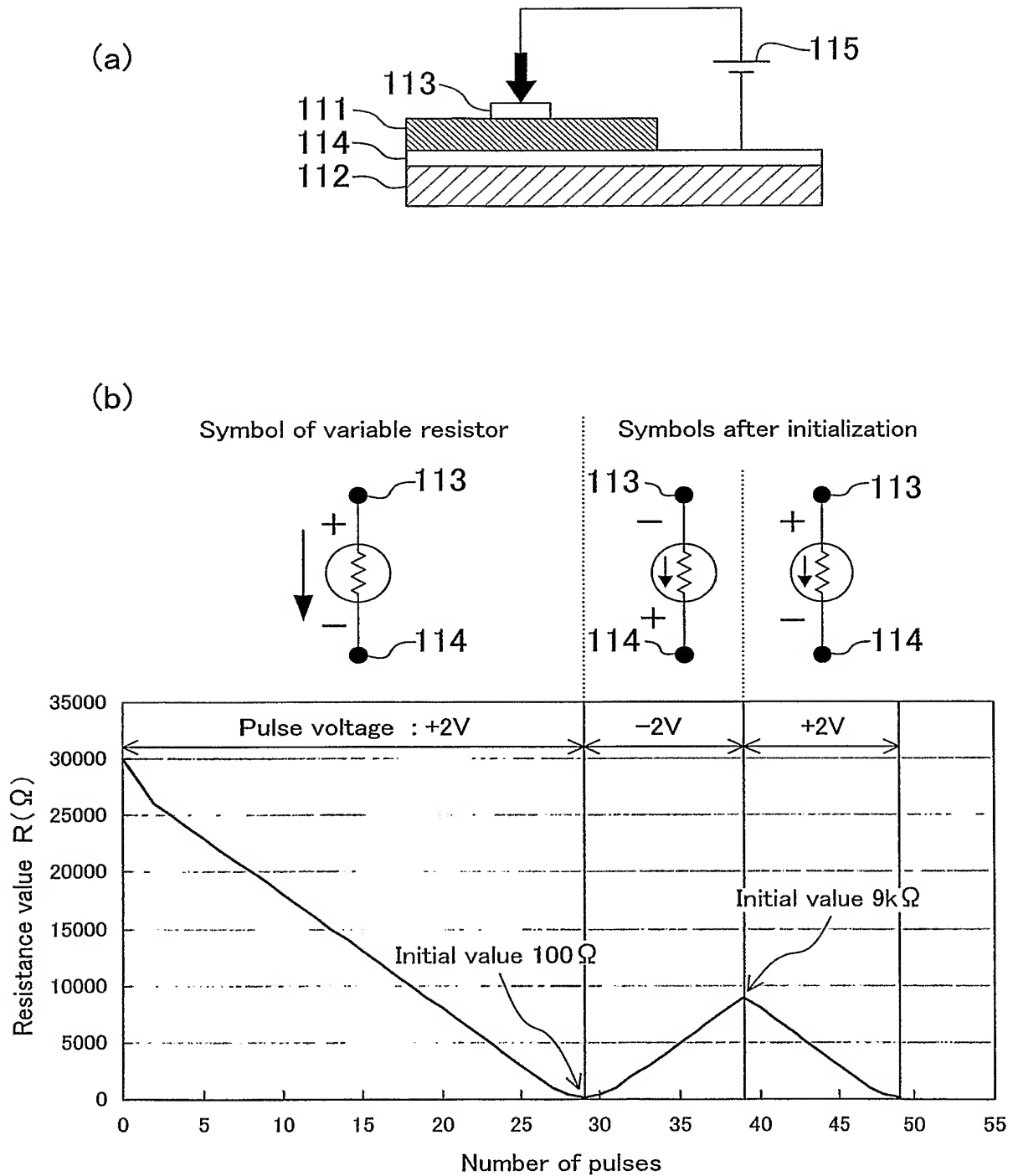
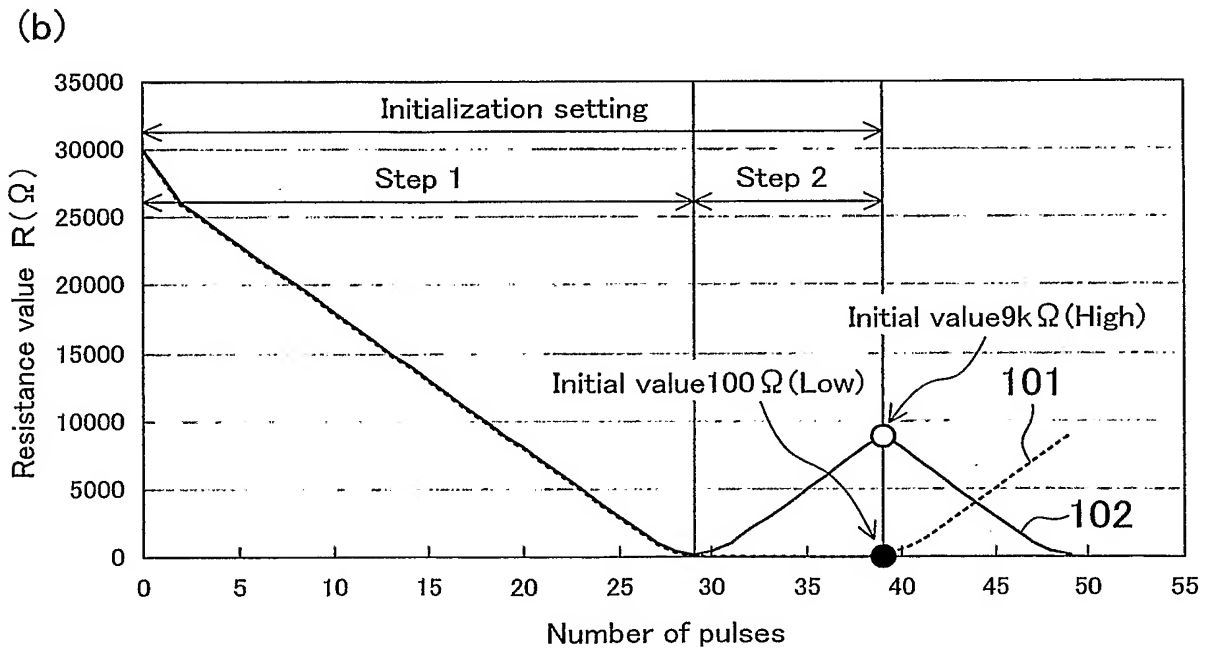
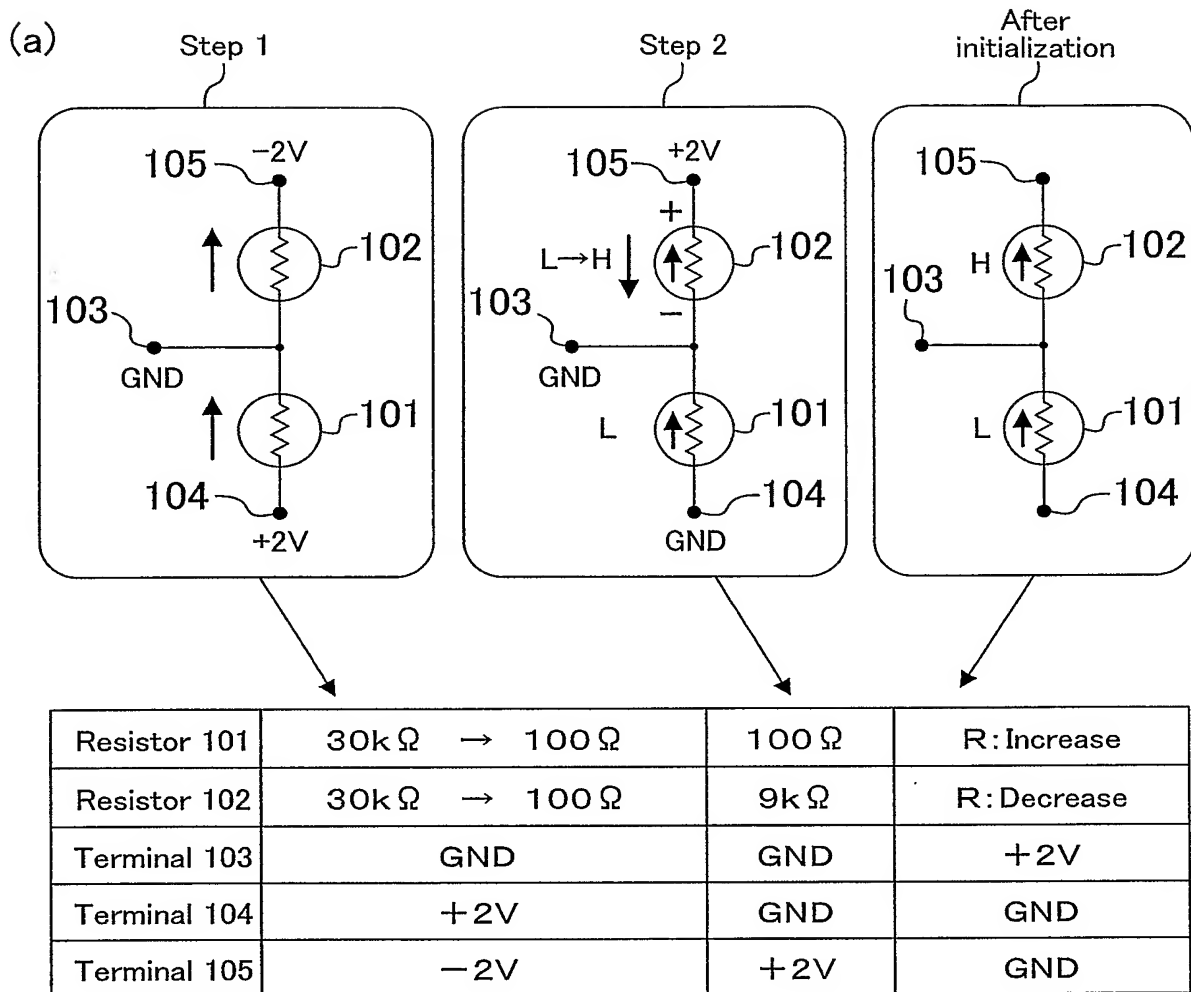
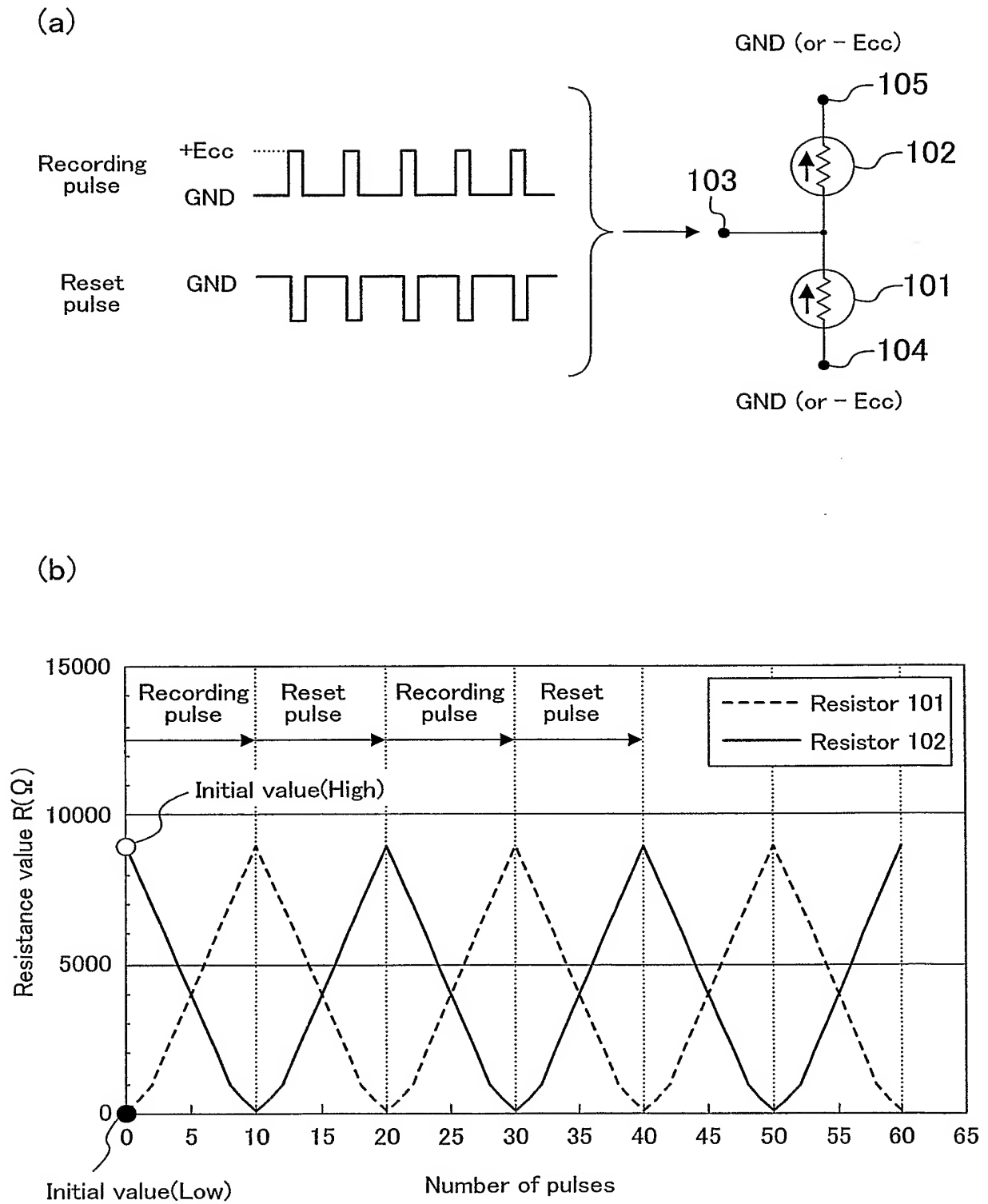


FIG. 30



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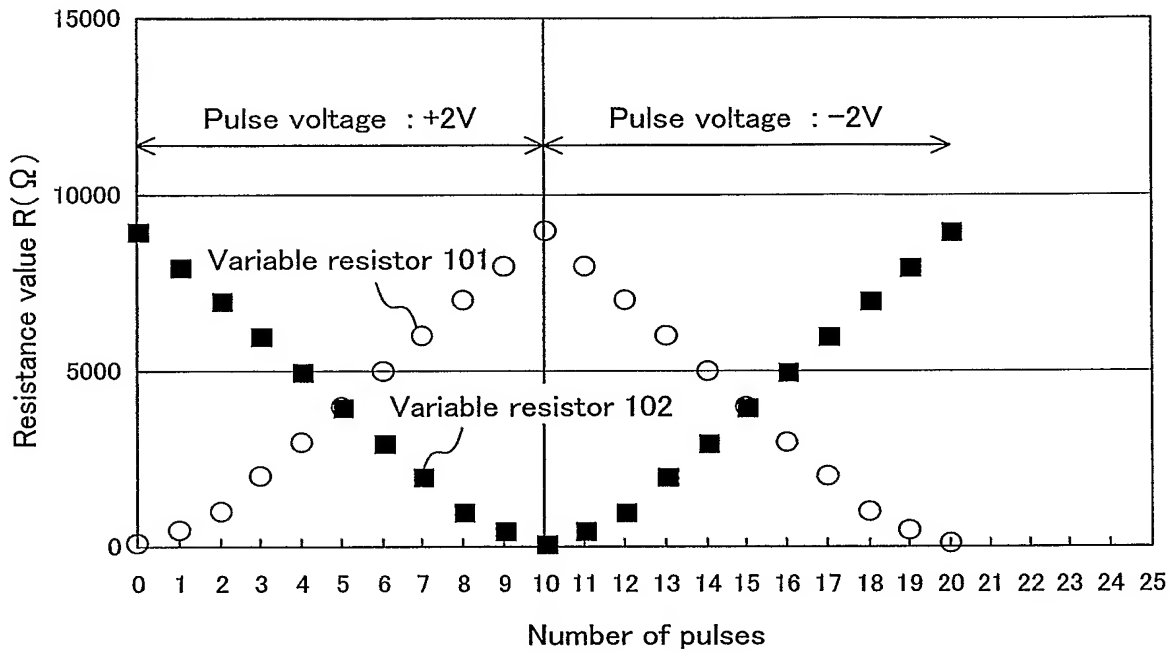
FIG. 31



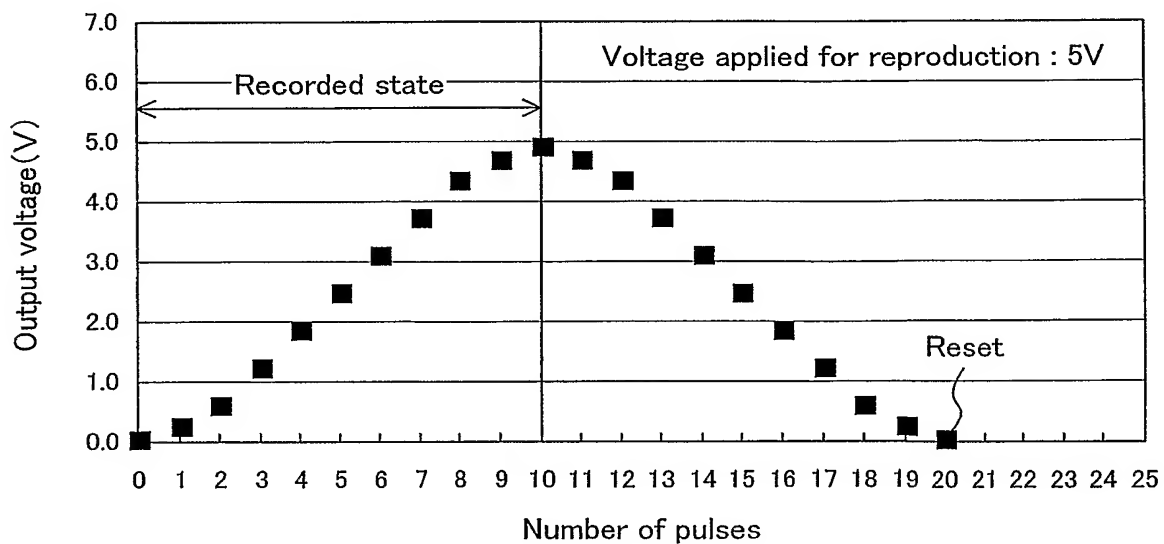
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FIG. 33

(a) Resistance variation over number of pulses



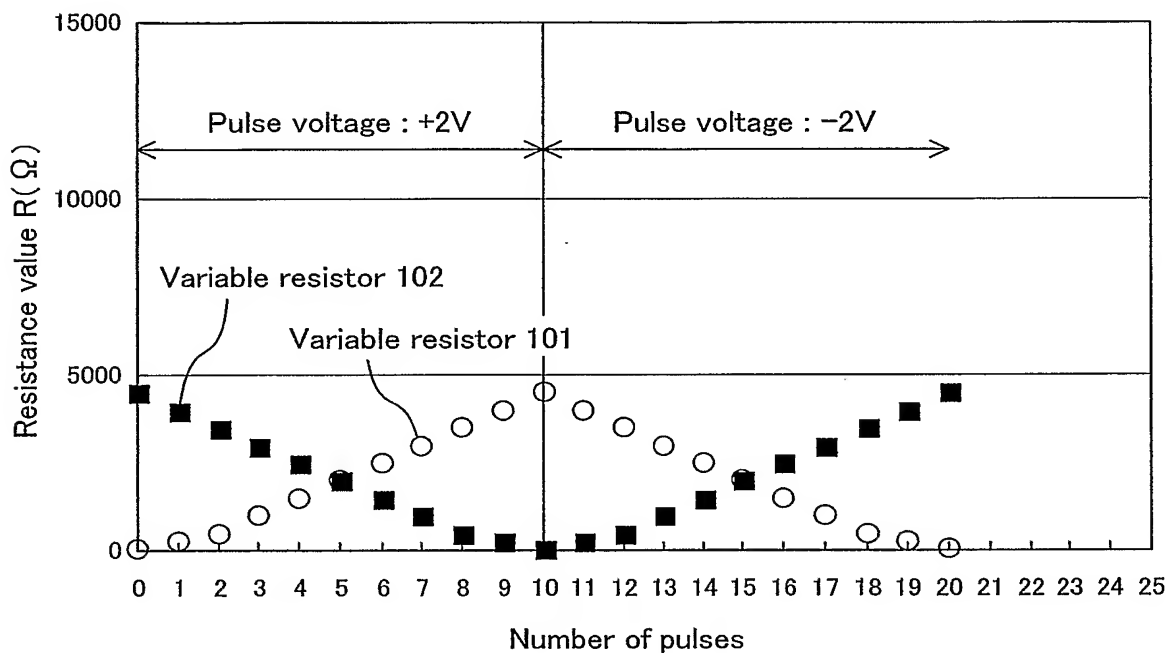
(b) Output voltage when reading recorded state



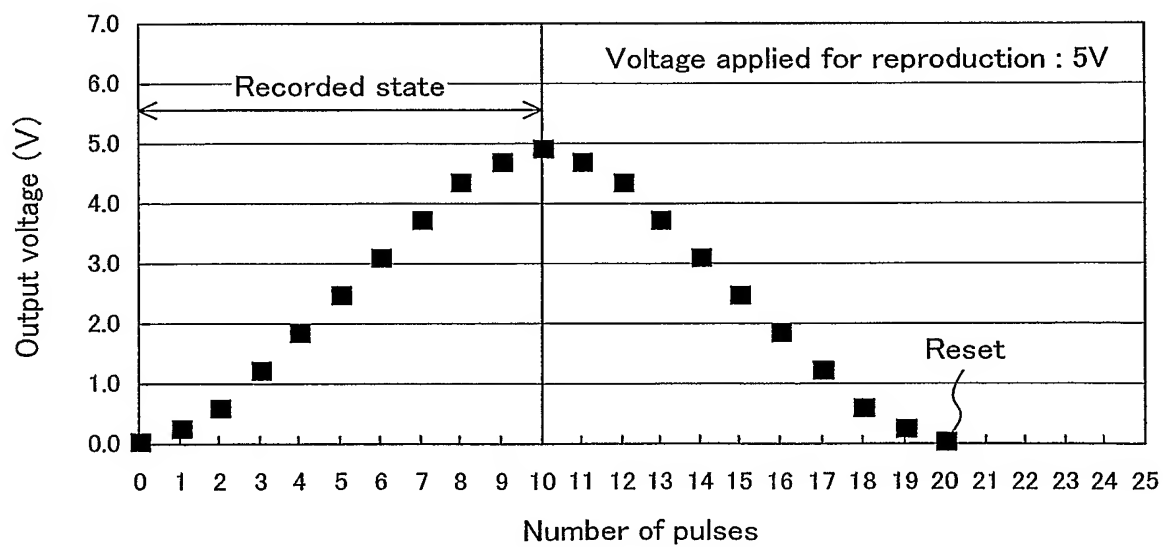
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FIG. 34

(a) Resistance variation over number of pulses

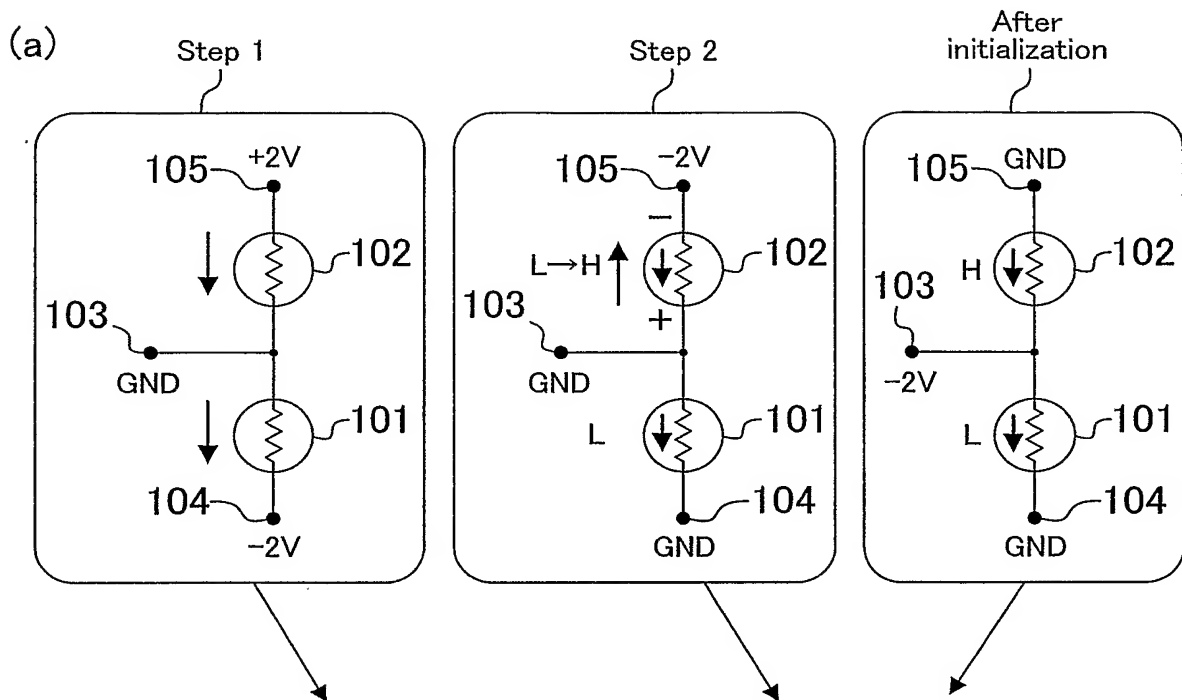


(b) Output voltage when reading recorded state



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FIG. 35



Resistor 101	$30\text{k}\Omega \rightarrow 100\Omega$	100Ω	R: Increase
Resistor 102	$30\text{k}\Omega \rightarrow 100\Omega$	$9\text{k}\Omega$	R: Decrease
Terminal 103	GND	GND	-2V
Terminal 104	-2V	GND	GND
Terminal 105	+2V	-2V	GND

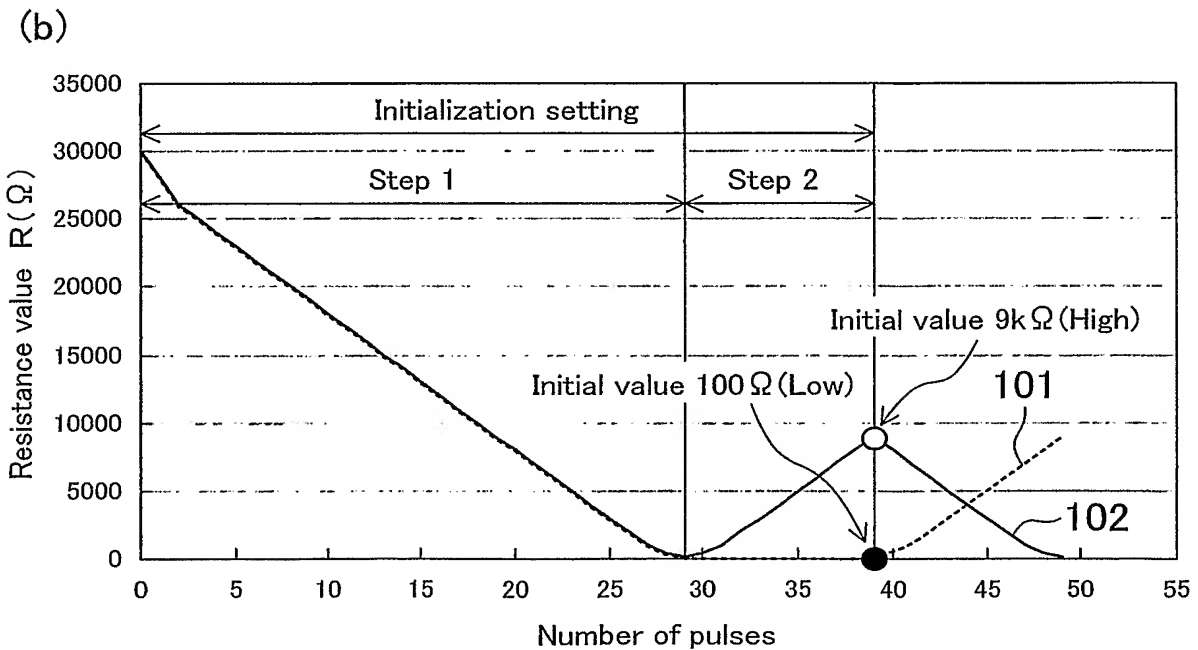


FIG. 36

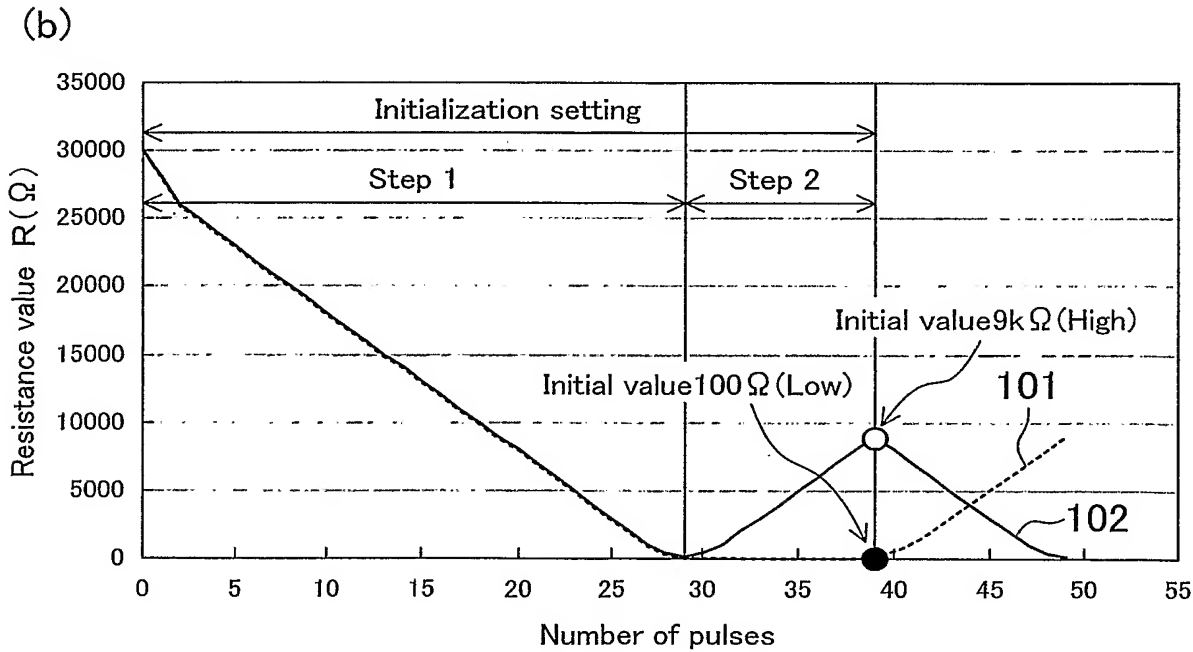
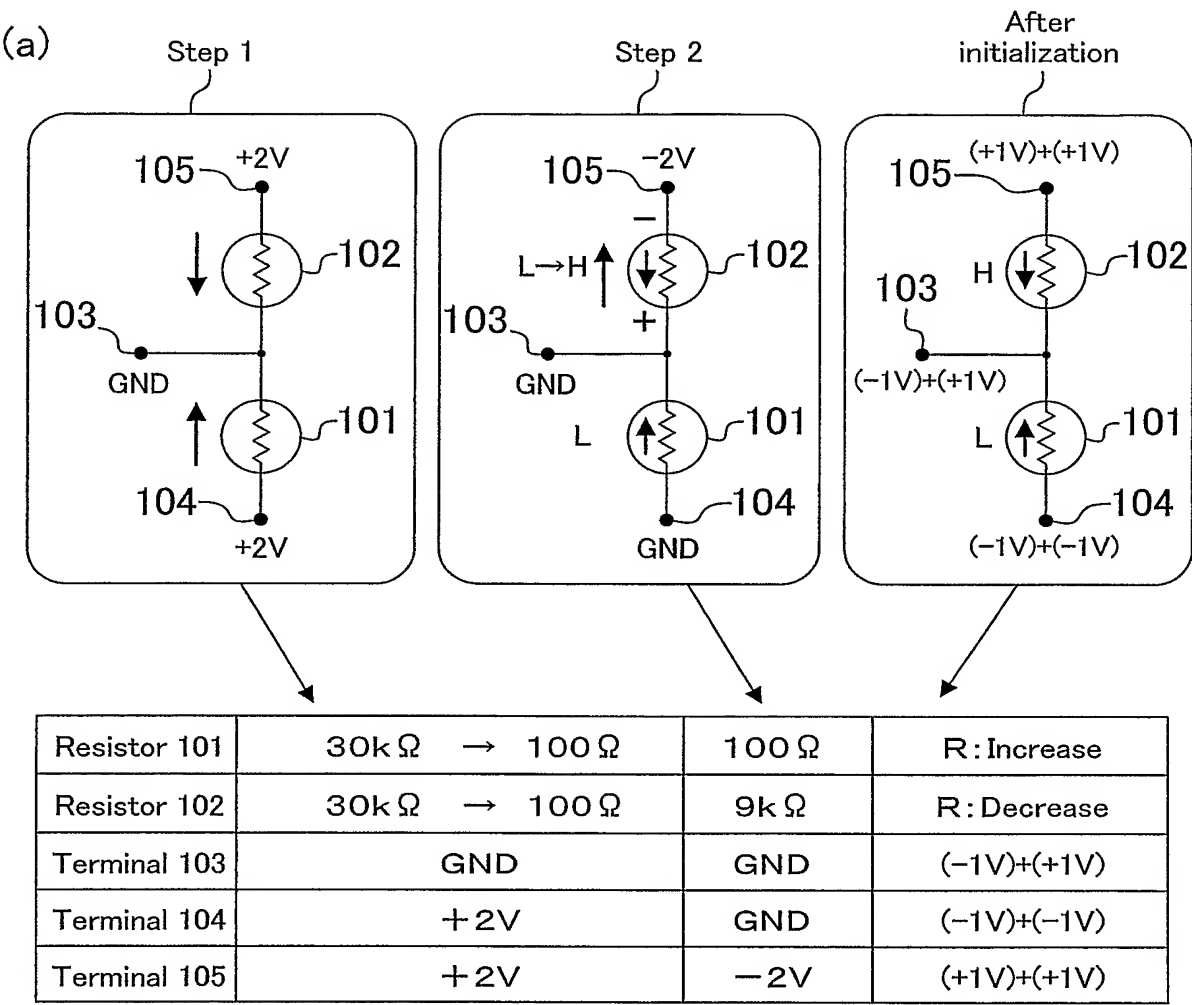
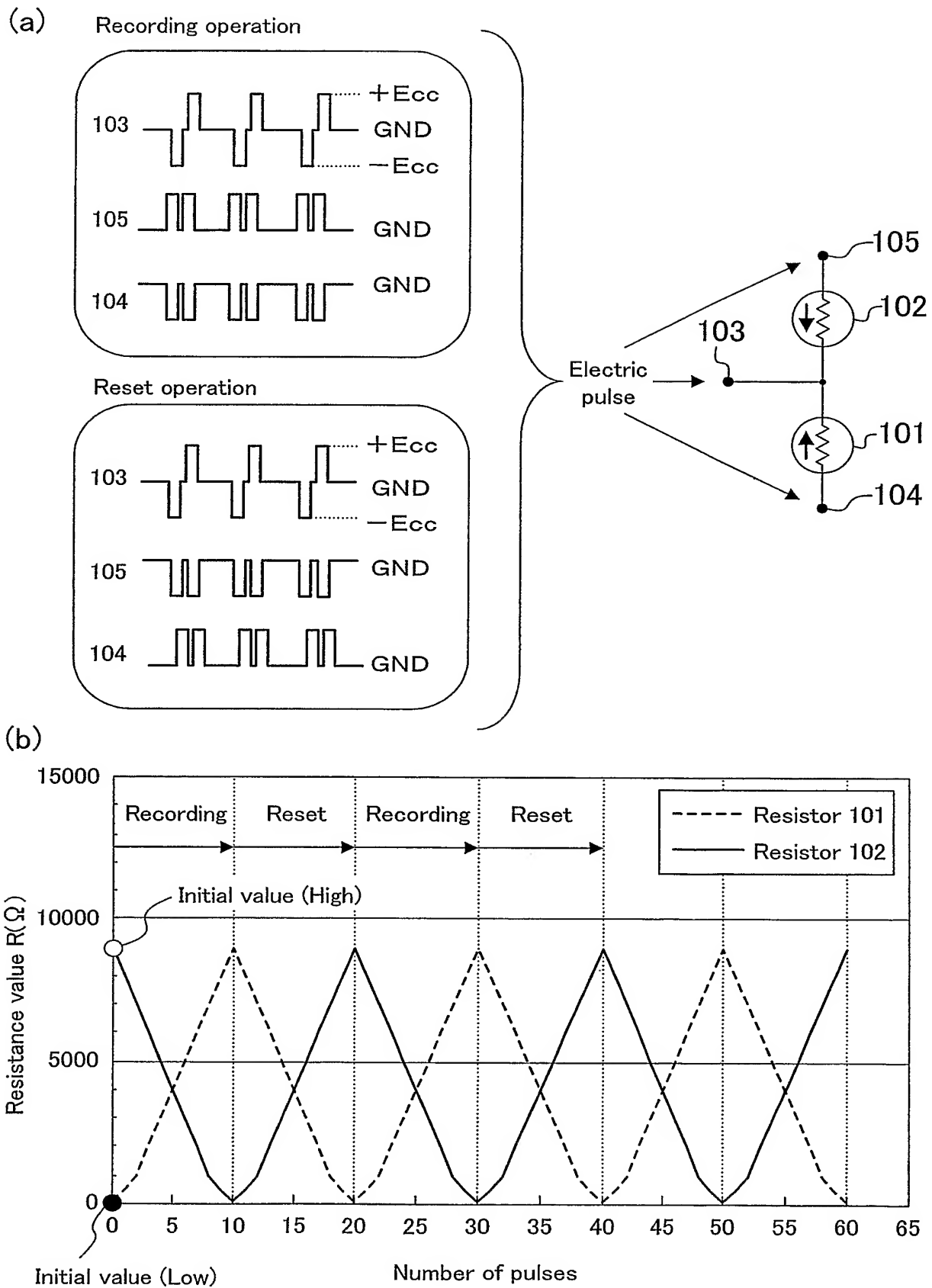


FIG. 37



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FIG. 38

